UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/045,041	03/20/1998	HISANORI FUJISAWA	122.1329	9340

21171 7590 05/29/2002

STAAS & HALSEY LLP
700 11TH STREET, NW
SUITE 500
WASHINGTON, DC 20001

EXAMINER
JONES, HUGH M

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 05/29/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09/045,041	Fujisawa
Examiner	**Art Unit**
Hugh Jones	2123

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Mar 20, 2002* .

2a) ☒ This action is **FINAL.** 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *9-12, 14-24, 26-36, and 38-44* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *9-12, 14-24, 26-36, and 38-44* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☒ All b) ☐ Some* c) ☐ None of:

1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Claims 9-12, 14-24, 26-36 and 38-44 of U. S. Application 09/045,041, filed 3/20/1998, are presented for examination.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

3. Claims 9-12, 14-24, 26-36 and 38-44 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Filseth or Yokomizo et al. or Chakrabarti et al..

4. Filseth discloses (abstract): "*The invention describes a method for expanding (flattening) hierarchical descriptions of electronic circuits into flat descriptions. The method is characterized by two processes: one which eliminates feed-through and implicit signals, and another which pre-plans the layout of the flattened data structure before flattening. The flattening process may then take advantage of a number of resulting efficiencies to operate more quickly than present flatteners.*"

- Col. 1, line 12 to col. 2, line 15 disclose: "Modern electronic systems are often designed with the assistance of electronic computer-aided-design tools, hereinafter referred to as ECAD tools. Typically, a user will capture a schematic diagram or other convenient form of circuit description on a display screen of an ECAD system using any of a number of interactive or automatic (e.g., module generators, silicon compilers, logic synthesizers) techniques widely known in the present art. As a part of the design process, a designer will typically capture and compile a design and then simulate it through the use of a logic simulator.

Complex logic circuits are customarily described hierarchically, but are simulated flat (or fully expanded). This means that if a module A in a user's design contains three instances of a submodule B, and submodule B contains two instances of another submodule C, the user will declare only two copies of submodule C in the process of capturing his design, but because of the implied replication in the user's design, the simulator will simulate six instances of submodule C for each instance of module A, since there are two instances of submodule C in each of the three instances of submodule B comprising module A. When such a circuit description is modified and re-simulated, a program must read the hierarchical description and produce a flat, or fully expanded, description of the hierarchical design before the simulation may be accomplished. A program that accomplishes this function is called a "linker" or "flattener". Hereinafter, the terms "link" and "flatten" will be used interchangeably. All modern ECAD systems include such a program, since a flat circuit description is too cumbersome for users to create directly, and a hierarchical description cannot easily be simulated directly, because the many different instances

of the submodules of a hierarchy may be in different states during simulation and must be dealt with individually by the simulator.

Inputs to a linker generally consist of a set of circuit descriptions of different hierarchical levels or "modules" in a circuit. Each module description contains a list of submodules, internal wires (also called "signals" or "nets") , and I/O (input/output) pins. Each I/O pin of the module's submodules is connected to one of the module's internal wires. Some of those wires are in turn connected to I/O pins of the module itself. The details of these interconnections are also a part of the module description. In addition, the module description contains the name of the module, the name of each submodule, internal wire, and I/O pin the module comprises. Any module may itself be a submodule of another module; further illustrating the impact of hierarchy on a design.

These inputs to the linker may be either memory-resident data structures, or data structures contained in files on an on-line mass-storage device. Since it is a relatively trivial process to move data structures between files and memory, it will be assumed hereinafter without loss of generality that all linker inputs are memory-resident.

The output from a linker is a flattened, or expanded, description of the input circuit descriptions. It contains an explicit representation of every copy of every bottom-level submodule in the circuit design. The term "bottom-level submodule" refers to submodules at the bottom level of a circuit hierarchy for which no further expansion is possible, i.e., submodules which comprise no further submodules. Hereinafter, such bottom-level submodules will be referred to interchangeably as "primitives". Each primitive has I/O connections (pins) which are

explicitly represented, but which may be replicated in multiple instances of the primitive. Connections between I/O pins of primitives may be made at a higher level of hierarchy where the details of the lower levels of circuit interconnection are not explicitly visible, but which do exist." See, also: col. 2, line 16 to col. 6, line 55.

5. Yokomizo et al. disclose "*A new circuit recognition and reduction method for pattern based circuit simulation.*" They further disclose a ***novel circuit recognition and reduction method to extract subcircuit data corresponding to the critical paths, including all relevant parasitics and internal loading. Circuit elements extracted from layout pattern data are combined to reconstruct logic gates, and a structure of the gates is recognized by the connection between the gate terminals.*** The recognized circuit data is reduced by tracing signal flows and picking up the gates along the specified critical paths. The circuit elements connected between a remaining net and an eliminated net are terminated as capacitive loads, and parasitic elements are merged or eliminated when the estimated error is permissible, compared with the specified error tolerance. The error is estimated by the first-order moment of the impulse response. Results on logic macrocells and memory peripheral control circuits show that the reduced circuit sizes are 15-50 times smaller, resulting in circuit simulation speedups of 50-300 times faster. See pp. 9.4.2-9.4.3.

6. Chakrabarti et al. disclose "*An improved hierarchical test generation technique for combinational circuits with repetitive sub-circuits.*" They also disclose an ***improved hierarchical testing algorithm for combinational circuits with repetitive sub-circuits using the bus fault***

model. This model exploits the regularity of a circuit by grouping together identical gate-level sub-circuits into high-level sub-circuits. Though the existing test generation techniques using this model reduces the required time substantially in many cases, it fails on encountering incompatibility between the inputs and outputs of high-level modules. The algorithm proposed helps in resolving high level incompatibility. The concept of a state transition graph has been used and it has been shown that resolving incompatibility at the high level is equivalent to finding a loop in the state transition graph. ***The technique is hierarchical in the sense that the original modeled high-level circuit is sub-divided into a number of components as soon as an incompatibility is encountered***. The results of implementation of the algorithm for a class of combinational circuits indicate a significant reduction in the test generation time and complete fault coverage thus validating our technique. See section 4.

7. Claims 9-12, 14-24, 26-36 and 38-44 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Hachiya.

8. Hachiya discloses a circuit partitioning apparatus comprising an update operation times ounting section that decomposes into the product of triangular matrixes the circuit matrix of each subcircuit composed of clusters generated by an initial clustering section; and a computation time prediction section that uses the results of counting by the update operation times counting section to predict simulation computation time required by a simulation execution time, prior to the execution of simulation, wherein the initial clustering section and a min-cut section feed back the results of the prediction section to carry out clustering and min-cut in order to create subcircuits

that require equal computation time for circuit simulation. Note fig. 2 (including a merge operation), fig. 5, fig. 7 (including a merge operation), fig. 8 and fig. 9 (merging of clusters prior to simulation).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 9-12, 14-24, 26-36 and 38-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shinsha et al. *or* Wang et al. *or* Kuehlmann et al..

11. Shinsha et al. discloses (abstract): "A logic design automation system examines correspondence relationship among sublogics in intermediate gate-level logic (containing neither physical design information nor manually optimized logic design information) produced from updated functional-level logic and current gate-level logic (containing the above information) to identify corresponding sublogics and non-corresponding sublogics of the gate-level logics with reference to primary input/output signals and input/output gates. For the corresponding sublogics, the corresponding sublogics of the current gate-level logic are selected, and for the non-corresponding sublogics, the non-corresponding sublogics of the intermediate gate-level logic are selected. The selected sublogics are combined to synthesize updated gate-level logic which

preserved therein the physical design information and the manually optimized logic design information for portions of the current gate-level logic which need not be modified."

Col. 1, line 49 to col. 2, line 8 disclose: "It is the object of the present invention to provide a novel method in a logic design automation system in which physical design information and manually optimized logic design information contained in portions of the current gate-level logic which need not be modified in updating the functional-level logic in the physical design phase are automatically succeeded to the updated gate-level logic. In accordance with the present invention, in a logic design automation system for automatically synthesizing gate-level logic from functional-level logic, the method comprises the steps of synthesizing intermediate gate-level logic containing neither physical design information nor manually optimized logic design information from the updated functional-level logic when portions of the current functional-level logic corresponding to the current gate-level logic containing the above information are modified, identifying corresponding sublogics and non-corresponding sublogics which are common and not common to the current gate-level logic and the intermediate gate-level logic, respectively, and combining the corresponding sublogics of the current gate-level logic with the non-corresponding sublogics of the intermediate gate-level logic to synthesize updated gate-level logic preserving physical design information and manually optimized logic design information for portions of the current gate-level logic which need not be modified." See, also: fig. 1-2, 6, 17; col. 5.

12. Wang et al. disclose, "*Restructuring binary decision diagrams based on functional equivalence*." The abstract discloses: "A method to restructure binary decision diagrams (BDDs) from a given input ordering to any other ordering is proposed. This technique is based on the concept of functional equivalence and BBDs structure equivalence. A transpositional operator is developed to implement the transformation. It is shown that this transformation is used to find a good input variable ordering for BBDs a good input partition for communication complexity based multilevel logic synthesis. Experimental results are presented. See, also: page 261 (functional and structural equivalence checking, structure modification); fig. 2 (structural equivalence); page 263 (Equivalence class, transpositional operator and variable ordering of BDD).

13. Kuehlmann et al. discloses, "*Equivalence checking using cuts and heaps.*" See: abstract; col. 1, pahe 263 (structural and functional equivalence); section 3 (merging of equivalent vertices). Also note fig. 2.

14. (Shinsha et al. *or* Wang et al. *or* Kuehlmann et al.) teach all of the limitations, but they do not explicitly teach simulation *before* device fabrication in order to verify functional and behavioral circuit characteristics. It would have been obvious to one of ordinary skill in the art at the time of the invention to carry out such a simulation because this is standard engineering practice - it would be costly and time consuming to fabricate a circuit which did not perform according to design specifications.

Response to Arguments

15. Applicant's arguments filed 3/20/2002 (paper # 22, entered as per RCE 3/20/2001) have been fully considered but they are not persuasive.

Response to Arguments - Claim Objections

16. The objection to the claims is withdrawn in view of the amendment (paper # 22).

Response to Arguments - 112(1) Claim Rejections

17. The 112(1) rejections are withdrawn in view of Applicant's arguments (pp. 3-4, paper # 22).

Response to Arguments - 112(2) Claim Rejections

18. The 112(2) rejections are withdrawn in view of Applicant's arguments (pp. 4-7, paper # 22).

Response to Arguments - Prior Art Claim Rejections

19. As per remarks (pg. 7, paper # 22) relating to the prior art rejections, the rejections are maintained. The Examiner again reminds Applicants that novel and non-obvious material was indicated during the interview (paper # 18). Furthermore, Applicants have not argued the patentable distinction between the amended claims and the disclosures in the prior art.

20. The arguments relating to the prior art rejections are identical to those offered on page 2 (paper # 15) and only state that "*...the Examiner has either repeated or modified his ... rejections from the prior Office Action. Applicants maintain their arguments...*". The Examiner had maintained, and continues to maintain, his previous arguments, as recited in paper # 20:

> *"" - Representative's arguments concerning the Filseth rejection (pp. 10-12, paper # 12), appear to be conclusary statements (regarding "different technology" or regarding claims of faster simulation speeds).*
>
> *- With respect to Representative's arguments concerning the Shinsha rejection (pp. 12-13, paper # 12), Shinsha discloses a logic design automation system examines correspondence relationship among sublogics in intermediate gate-level logic (containing neither physical design information nor manually optimized logic design information) produced from updated functional-level logic and current gate-level logic (containing the above information) to identify corresponding sublogics and non-correspondingsublogics of the gate-level logics with reference to primary input/output signals and input/output gates.* ***For the corresponding sublogics, the corresponding sublogics of the current gate-level logic are selected, and for the non-corresponding sublogics, the non-corresponding sublogics of the intermediate gate-level logic are selected. The selected sublogics are combined to synthesize updated gate-level logic which preserved therein the physical design information and the manually optimized logic design information for portions of the current gate-level logic which need not be modified.***

- With respect to Representative's arguments concerning the Wang rejection (pg. 13, paper # 12), see pg. 261 (Wang).

- With respect to Representative's arguments concerning the Kuehlmann rejection (pg. 13, paper # 12), see section 2 (Kuehlmann).

- In response to applicant's arguments againstthe references individually (pp. 11-13, paper # 12), one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See In re Keller, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); In re Merck & Co., 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986)."

28. Applicant's arguments against the Yokomizo et al., Chakrabarti et al., Hachiya and Fujisawa rejections (pp. 3-4, paper # 15) are not persuasive.

29. Yokomizo et al. disclose "*A new circuit recognition and reduction method for pattern based circuit simulation.*" They further disclose a ***novel circuit recognition and reduction method to extract subcircuit data corresponding to the critical paths, including all relevant parasitics and internal loading. Circuit elements extracted from layout pattern data are combined to reconstruct logic gates, and a structure of the gates is recognized by the connection between the gate terminals.*** The Examiner has reviewed Applicant's arguments (paragraph 5 [i.e., "Thus, the Yokomizo..."], page 3, paper # 15) and respectfully does not agree with Applicant's assertion that there is a patentable distinction between the prior art and Applicant's claimed invention - as argued in this paragraph.

30. The Examiner has reviewed Applicant's arguments (last paragraph, page 3, paper # 15) and respectfully does not agree with Applicant's position concerning Chakrabarti et al.. They disclose "*An improved hierarchical test generation technique for combinational circuits with repetitive sub-circuits.*" They also disclose an ***improved hierarchical testing algorithm for***

combinational circuits with repetitive sub-circuits using the bus fault model. This model exploits the regularity of a circuit by grouping together identical gate-level sub-circuits into high-level sub-circuits. The technique is hierarchical in the sense that the original modeled high-level circuit is sub-divided into a number of components as soon as an incompatibility is encountered. See section 4.

31. The Examiner has reviewed Applicant's arguments (second full paragraph, page 4, paper # 15) and respectfully does not agree with Applicant's position concerning Hachiya. Note fig. 2 (including a merge operation), fig. 5, fig. 7 (including a merge operation), fig. 8 and fig. 9 (merging of clusters prior to simulation). The Examiner respectfully does not agree with Applicant's assertion that there is a patentable distinction between the prior art and Applicant's claimed invention - as argued in this paragraph.

32. The Examiner has reviewed Applicant's arguments (third full paragraph, page 4, paper # 15) and respectfully agrees with Applicant's position concerning Fujisawa. The Fujisawa rejection is withdrawn."

Conclusion

21. All claims are drawn to the same invention claimed in the application prior to the entry of the submission under 37 CFR 1.114 and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the application prior to entry under 37 CFR 1.114. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action after the filing of a request for continued examination and the submission under 37 CFR 1.114. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

22. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

23. Any inquiry concerning this communication or earlier communications from the examiner should be:

directed to:

Dr. Hugh Jones telephone number (703) 305-0023, Monday-Thursday 0830 to 0700 ET, ***or*** the examiner's supervisor, Kevin Teska, telephone number (703) 305-9704. Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist, telephone number (703) 305-3900.

mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 308-9051 (for formal communications intended for entry)

or (703) 308-1396 (for informal or draft communications, please label "*PROPOSED*" or "*DRAFT*").

Dr. Hugh Jones
May 28, 2002

DR. HUGH M. JONES
PATENT EXAMINER
ART UNIT 2123